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A Two Stage AC-DC Converter For Speed Control Of A DC Motor

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Abstract—In this paper a AC-DC converter has been proposed for the application of speed control of a DC motor. The converter comprises two stages. The first stage is the diode bridge rectifier and the second stage is DC-DC buck converter. The two stages are coupled by a dc-link capacitor which also eliminate the ripple present in the output of the rectifier. For DC-DC buck converter, a feedback control system, based on PWM technique, has been designed which regulates its output to control the speed of dc motor. The prototype model has been designed and results obtained with it have a closed resemblance with the simulation results which has been done in LTspice software. The results of the simulation and prototype demonstrate that the output voltage of DC-DC converter and hence the speed of the dc motor can be controlled by controlling the duty cycle of DC-DC converter. The results also demonstrate the faster dynamic response of the converters.

Index Terms—AC-DC Converter, continuous conduction, dc-dc converter, feedback control, pulse width modulation (PWM).

I. INTRODUCTION

Day by day, application of single phase ac to dc conversion system are increasing with the increasing requirements for dc power. Most of the applications requires power ranging from 12V to 400V of dc supply. A large number of applications involves the use of dc motors. Therefore, it is necessary to have a efficient power conversion system.

Here, the designed two stage ac to dc converter is unidirec- tional and is used to control the speed of a dc motor. To control the speed of motor, the output of the buck converter must be regulated, which can be achieved by an efficient feedback control loop. However, the design of an efficient feedback loop is not easy as its performance is significantly affected by the disturbances. These disturbances are basically created by load variations, changes in input voltage, and electromagnetic interference, which is caused by the switching operations of semiconductor devices such as MOSFETs, transistors and diodes [1], [2]. Therefore, to obtain the desired output voltage, the feedback control system must have a high disturbance rejection ability.

Many researchers have proposed different control schemes such as predictive control [3], adaptive control [4], sliding mode control [5] and fuzzy logic control [6] which lead to improvement in performance of feedback control system.

In this paper, authors have implemented PWM control tech- nique because of its simplicity. Also, to achieve the high conversion efficiency, the efficiency of rectifier as well as dc-dc converter should be high. Therefore, in the proposed model, fast recovery diodes has been used in the dc-dc converter which result in reduced voltage drop across diode and hence, increased converters efficiency. The lower value of selected switching frequency also results in lower switching losses and further increases the buck converter efficiency.The control method, dc capacitor design and ac inductor design are discussed in this paper. Supplying other components of the circuit like ramp generator, amplifier and comparator, which operates at low-voltage, from the output of the rectifier is the another concern of this paper.

The paper is organized as follows. Section II gives the de- scription of complete topology for ac to dc conversion system. Section III contains the components used along with their size calculations. Section IV and V consists of simulations and experimental results respectively followed by conclusion in section VI.

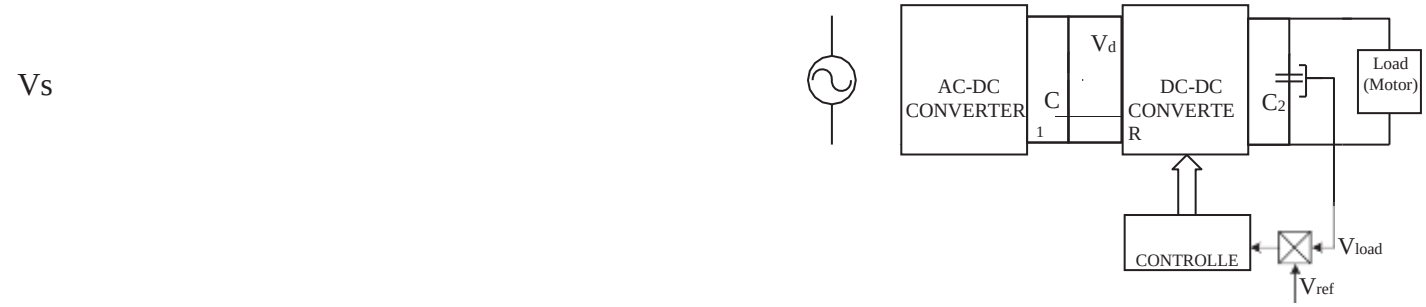

Fig. 1: Block diagram of complete conversion system

II. II. TOPOLOGY DESCRIPTION

A. Front end AC-DC Conveter

In this paper, the single phase ac to dc conversion system basically consists of two stages. The first stage is full bridge rectifier which converts the ac input from the main supply into dc and is widely used in many previous designs. Since the

front end rectifier is operating at power frequency, i.e 50Hz, switching loss is not an issue for it. The ripples present in the output of the full bridge rectifier is minimized by placing a capacitor at the output of rectifier. The size of the capacitor has been determined in section III.

B. DC-DC Buck Converter

The second stage is a dc to dc buck converter which consists of an inductor L_1, a filter capacitor C_2, a switch, and a diode D_5. The output of the converter is given to the dc motor. The switching frequency is $f_s = \frac{1}{T}$ and duty cycle is D. The converter is operating in continuous conduction mode by selection of suitable value of inductor. The size of the inductor has been determined in section III.

C. Feedback Control

To efficiently control the output of buck converter, a high- performance feedback controller for dc-dc switched converter system is needed which have high disturbance rejection ability, smaller steady-state error, faster dynamic response, and lower overshoot. In this paper, PWM technique is used to control the switching of semiconductor device. A type III compensator is used in the feedback loop which generates the error signal by comparing the feedback voltage to the reference voltage. The comparator compared this error signal with the signal obtained from ramp generator. If the magnitude of error signal is more than ramp signal, then the output of comparator will be high and vice versa. Therefore, the output voltage of the control circuit produces pulses, with a duty cycle 'D' varying from 0 to 1, which control the switching action of the switch of converter. The frequency of the ramp signal determines the frequency of the comparator output which is the frequency of the converter [7].

The various components of feedback control system is de- scribed below:

1) Compensator: : The compensator circuit is shown in Fig.

2. A type III compensator (lead compensator) is used in our design. The design demonstrated in this paper uses a simple error amplifier to provide rudimentary feedback, achieving closed-loop control of the buck converter. To improve output stability and response to changing load, a compensator should be implemented as an enhancement to the original design.

The topology of the buck converter gives it a characteristic frequency response; two complex conjugate poles from the L- C circuit formed by the output filter, and a single zero from the R-C circuit formed by the output capacitor and its parasitic equivalent series resistance (ESR).

The desired closed-loop frequency response should have high gain at DC and decreasing gain with increasing frequency rejecting high-frequency noise and ripple due to the switch- ing characteristic of the DC-DC converter. Additionally, the closed-loop phase response should have high phase margin for closed-loop stability. A type III compensator is suitable for providing two poles and three zeroes to shape the magnitude and phase response to meet these requirements.

The Placement of poles and zeroes of the compensation network aims to nullify the effect of the poles and zeroes of the uncompensated buck converter, producing the desired linear roll-off response. Design of a type III compensator is heavily reliant on the inductance, capacitance, and resistance of the filter components of the buck converter design.

The complex conjugate pair of resonant poles f_o and ESR zeroes f_{esr} of the buck converter's output filter is given as:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

$$f_{esr} = \frac{1}{2\pi RC} \quad (2)$$

Type III Compensator Design Procedure: The type III compen- sator generates three poles and two zeroes, with one implicit pole at DC. The zero f_{z2} is placed at the resonant frequency of the LC filter f_o and another zero f_{z1} at $\frac{f_o}{}$. These zeroes compensate for the −40dB per decade roll-off introduced by the resonant poles. The positioning of f_{z1} is chosen to prevent the phase response from approaching −180 at f_o, which would otherwise occur if f_{z1} and f_{z2} occupied the same frequency. The remaining two poles are placed relative to f_{esr} to compensate

the ESR zeroes; f_{p1} is placed at f_{esr}, and the so-called closure pole f_{p2} between $3f_c$ (the crossover frequency) and $\frac{fsw}{}$. The result of this compensation is that the closed-loop response of the switching DC-DC converter has a 20dB per decade roll-off, and 40dB per decade beyond the ESR zeroes. The design requirements for pole-zero locations

are summarised below.

$$f_{z1} = \frac{f_o}{2} \quad (3)$$

$$f_{z2} = f_o \quad (4)$$

$$f_{po} = 0 \quad (5)$$

$$f_{p1} = f_{esr} \quad (6)$$

$$3f_c \leq f_{p2} \leq \frac{fsw}{2} \quad (7)$$

The complete transfer function of the type III compensator is given by Lee [8]:

$$Hs = \frac{(sC_2(R_1 + R_3) + 1)(sC_1R_2 + 1)}{(sR_1(C_1 + C_3))(sC_3R_2 + 1)(s\frac{C_1C_3R_2}{} + 1)} \quad (8)$$

Making the simplifying assumption that $C_1 \ll C_3$, Lee [8] derives design equations for the R C networks that form the compensator:

$$R_2 = \frac{R_1f_{po}f_{p2}}{(f_{p2} - f_{z2})f_{z2}} \quad (9)$$

$$R_3 = \frac{R_1f_{z1}}{f_{p1} - f_{z1}} \quad (10)$$

$$C_1 = \frac{f_{p2} - f_{z2}}{2\pi R_1f_{po}f_{p2}}$$

$$C_1 = \frac{f_{p1} - f_{z1}}{}$$

(11)

(12)

2piR1fp1fz1

$$C_3 = \frac{f_{z2}}{2\pi R_1 f_{po} f_{p2}}$$

(13)

2) Ramp Generator: :The function of the ramp gener- ator is to produce a reference sawtooth-wave at a fixed-frequency. The common 555 timer can be used to design a simple oscillator circuit known as an astable multivibrator, and with some modifications can generate the sawtooth signal. A constant-current source is formed by transistor Q4 and resistors R18, R19, R20, charging capacitor C5. Since the rate of change of voltage across a capacitor is proportional to current, the voltage developed across C5 increases linearly
voltage source capable of producing 5V in order to scale the sawtooth-wave output to between 0 and +5V . The frequency of the signal generated by ramp generator is given as:
which is mathematically expressed as:

$$f_s = \frac{dV(t)}{C(V_{CC}/3 + 0.4)}$$

(15)

$$I_C(t) = C \frac{I_C}{Dt}$$

(14)

where, V_{CC} is the regulated voltage by zener diode at the

where, I_C is the current through the capacitor.

output of rectifier.
Once the voltage across C5 reaches $\frac{2}{3}$
of the supply volt-
age to U 3, the discharge pin is pulled low, discharging the voltage across C5 via R21, which protects the open-collector discharge pin of U 3 from excessive current. When the voltage

3) Charge Pump:: An inverting charge pump is used to
generate the negative supply required for the correct operation of the ramp generator. This circuit is also constructed from
across C5 is reduced to $\frac{1}{3}$
of the supply voltage to U 3,
a 555 timer, which operates as an astable-multivibrator in a

the open-collector output is cut-off and C5 begins to charge again. This circuit relies on the availability of a negative voltage-controlled oscillator configuration. The output of the
astable-multivibrator is a square wave, which charges capacitor C7 through diode D7. When the output of U 2 goes low, the voltage previously developed across C7 produces a negative voltage at the cathode of D8, which begins conducting to share the charge between C7 and C8. Capacitor C8 provides output filtering and charge storage for the negative supply output.
Regulation of the output voltage is performed through voltage- control of the oscillation frequency. This is achieved by manipulating the voltage at the control pin via feedback of the output voltage to the base of transistor Q5, which affects the high and low comparator thresholds where the discharge pin is switched between 0V and high-impedance output.

4) MOSFET Driver: The circuit of the MOSFET gate driver is shown in Fig. 2 inside dotted line. The MOSFET driver is designed to source and sink current to charge and discharge the capacitance of the gate as quickly as possible, reducing the period that the MOSFET is conducting in the linear region of operation, and reducing switching losses. A P channel field-effect transistor (FET) was selected for the high- side drive topology since this simplified the driver circuitry

compared to an N channel FET.
Transistor Q3 is responsible for providing the high-current gate drive for charging and discharging the gate capacitance of M 1. Q3s bias network (R7, R8) set the gate voltage to approximately 15V below V_d when Q3 is in the active region, and equal to V_d when Q3 is in cutoff. The 15V zener diode D5 is included to ensure that the gate-source voltage V_{gs} of M 1 does not exceed the maximum gate-source voltage $V_{gs(max)}$, which is 20V for the chosen MOSFET. Capacitor C2 at the emitter of Q3 is included to speed up the discharge of the gate capacitance of M 14 when Q3 is turned on.
Transistors Q1 and Q2 are configured as inverting level- shifters. Q1 provides the voltage amplification required to turn on Q3 from a 5V logic-level PWM signal, and Q2 compensates for the signal inversion produced by Q1, so that a positive input voltage from the PWM generator causes the MOSFET to conduct.

III. COMPONENTS USED

The complete list of components used in our prototype model and their costs are mentioned in appendix. The value and specification of some important components are listed in Table-1.

A. Choice of inductor

To operate the dc-dc converter in continuous conduction mode, inductor value should be higher than its value just at the boundary of continuous and discontinuous mode. At the boundary of continuous and discontinuous mode, the inductor current i_L goes to zero at the end of the off period. Therefore,

B. Choice of capacitor

The energy stored in a capacitor is given as:

$$Q = CV \tag{18}$$

Therefore, the energy discharge through the capacitor will be equal to capacitance times the capacitor voltage ripple and hence, mathematically expressed as:

$$\Delta Q = C\Delta V \tag{19}$$

The energy discharge through the capacitor can also be given as:

$$\Delta Q = I_{in}\Delta t \quad (20)$$

where, I_{in} is the input current through capacitor and Δt is the time for which capacitor discharges which is half of the time period of input supply. Therefore, for 50Hz supply, Δt will be $\frac{1}{100}$ seconds.

Now, ideally dc-dc converter should not dissipate any power and output power (P_{out}) must be equal to input power (P_{in}), but practically, some power get dissipated by the circuit components and hence, the efficiency get reduced. In this paper, the targeted efficiency for dc-dc converter is 80%.

$$P_{out} = 0.8 * Pin \quad (21)$$

$$V_o I_o = 0.8 * V_{in} I_{in} \quad (22)$$

Converter's output current is equal to the full load current of the motor taken i.e 80mA. Using the known values for V_o, I_o and V_{in}, I_{in} can be easily calculated using equation (7).
Then, using equation (4), (5) and (7), the capacitor value ca
at the boundary, the average inductor current I_{LB} can be given be calculated as:

I Δt

as:

$$I_{LB} = \frac{1}{2} i_{L,peak} = \frac{t_{on}}{DT_s}(V_o - V_{in}) = \frac{DT_s}{2L}(V_o - V_{in}) \quad (16)$$

$$C = \frac{\Delta I_{in}}{\Delta V} \quad (23)$$

IV. SIMULATION RESULTS

where, $i_{L,peak}$ is the peak value of inductor current, t_{on} is the time for which the switch remain in ON position, L is the inductance of inductor and D is the duty cycle of converter. Therefore, using the equation (1), following condition must be satisfied for continuous conduction operation of converter:

$$L \geq \frac{DT_s}{2L}(V_o - V_{in}) \quad (17)$$

In the simulation model, an input supply of 33.94V is given to the rectifier. The rectifier output is measured to be 32V dc with very less ripples i.e 680mV because of the filter action. The rectified voltage is given to dc-dc buck converter which, by the controller action, gives the output voltage in the range of 9V to 24V. Also, in the simulation model, instead of motor load, a resistance equivalent to motor load has been used.

In Fig. 7, V (des) and V (vo) are the reference and actual output voltage of dc-dc converter respectively and the blue color waveform is the PWM signal. It clearly demonstrate the wide duty-cycle range of the controller. Also, during each transition, the controller takes less than 2ms to follow the reference which shows its fast reference-

tracking response. The zoom in view of PWM signal along with ramp and control signals for 30% and 70% duty cycles are shown in Fig. 8 and Fig. 9 respectively. These results show the effective variation in the width of PWM signals with the duty cycle.

V. EXPERIMENTAL RESULTS

In our prototype model, as shown in Fig. 10, the ac supply from the mains is given to the full bridge rectifier by a power pack which steps down the 240V ac into a 24V ac. The list of all the components used in making the model and their costs are mentioned in appendix. The average output voltage of bridge rectifier is 35.8V , shown by green waveform in Fig. 11, with ripple value 2.4V . The ramp signal and the output of compensator i.e control signal are shown by blue and red waveforms in Fig. 12. The output of dc-dc converter is shown in Fig. 13 and the obtained results demonstrate that the output
voltage converges to the reference voltage in the finite time. The conversion efficiency can be calculated as:

$$\eta system = \eta rectifier * \eta dc{-}dc \quad (24)$$

VI. CONCLUSION

In this paper, a two stage ac-dc converter has been im- plemented for a wide range of dc voltage. The dc output of rectifier with ripples in the range of milli-volts shows its high efficiency. The operation of buck converter at low switching frequency along with the use of fast recovery diode results in increase in its efficiency. Moreover, instead of using an external dc supply to the components in the feedback loop, a charge pump has been incorporated into circuit which further improves the over all efficiency of system. The applied PWM technique results in getting wide range of output voltage by varying duty cycle. In addition to that, the disturbance rejection ability and fast dynamic response of controller result in accurate and fast tracking of reference voltage.

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